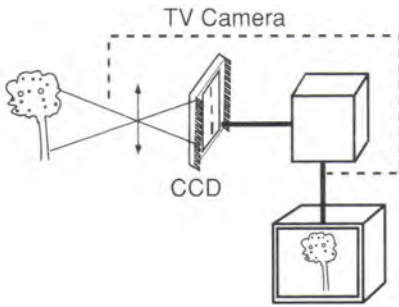# THE CCD
IMAGE SENSOR

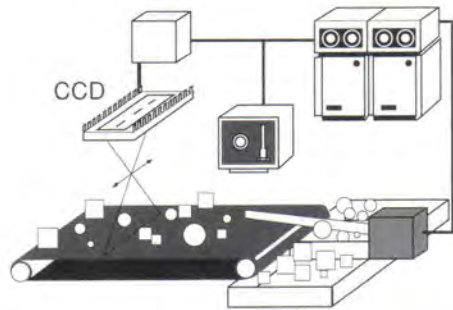**THOMSON COMPOSANTS
MILITAIRES ET SPATIAUX**

THE CCD IMAGE SENSOR

INTRODUCTION

In its broadest definition, a charge-coupled device (CCD) image sensor is an analog integrated circuit that converts an optical image into an electronic output - in other words it is the electrooptic interface in an electronic image pickup system.

CCDs are among the fastest growing family of components in electrooptics. As with many semiconductor components, their evolution from a laboratory concept (in 1970) has been a rapid one, boosted by their potential for a wide range of applications in both consumer products and sophisticated professional equipment.

Much of the success of CCDs rests on the fact that they are conceptually very simple and come in the form of MOS integrated circuits. Indeed, their integrated nature provides their best known features : unlimited lifetime, low power drain, miniaturization, ruggedness and immunity to image burn-in, to name but a few. To these we can add some more specific characteristics, including : image analysis in discrete elements (pixels) with exact field registration and a sampled output signal delivered at low impedance.

This short guide introduces the basics of CCDs and their electrooptical characteristics, and should give adequate background information to engineers and technicians called to work with these fascinating devices.

CONTENTS

PART V - CCD IMAGE SENSOR PERFORMANCE :
Definitions and Measurement Principles

V.1 - ELECTRICAL PERFORMANCE

V.2 - ELECTROOPTICAL PERFORMANCE

PART I
BASIC CCD THEORY

Throughout the following discussion it will be useful to note that CCDs handle electrical charges in a maner closely analogous to a hydraulic system, i.e. charge packets can be regarded as quantities of fluid stored and shifted in a series of buckets.

I.1. - HOW DOES A CCD IMAGE SENSOR WORK ?

A CCD image sensor operates in four successive steps :

- during the exposure period

a) it converts the incident illumination into a proportional quantity of electrical charges (photocharges). This is achieved by an array of photoelements disposed either along a line (linear array) or in a two dimensional matrix (area array) ;

b) it stores the photocharges from each photoelement in an associated MOS capacitor (potential well)
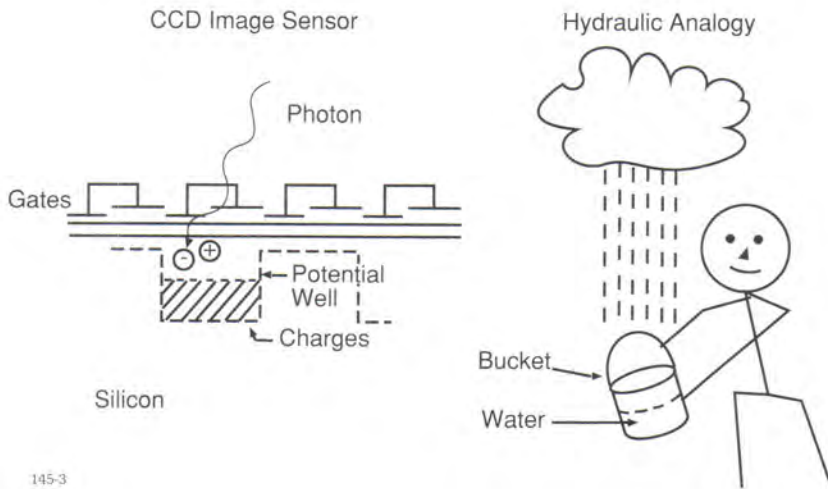
Figure 1 - The hydraulic analogy

- after the exposure period.

c) it transfers the accumulated photocharge packets sequentially along the MOS capacitors to a readout stage (here, the CCD acts as an analog shift register) ;
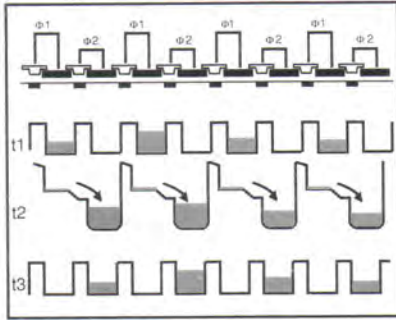
Figure 2 - Charge transfer along the MOS capacitors

d) at the readout stage, each arriving photocharge packet is converted into a proportional voltage signal. Additional sampling and amplification give the low impedance output video signal.
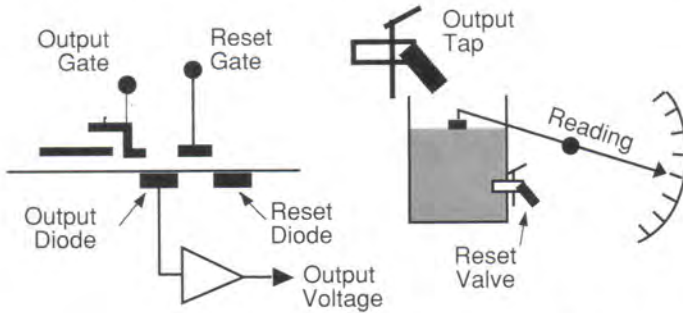
Figure 3 - Charge-to-voltage conversion at the readout stage

A CCD image sensor can thus be considered as a "black box" which transforms an optical image, i.e. a spatial distribution of radiation, into a time-distributed voltage signal.
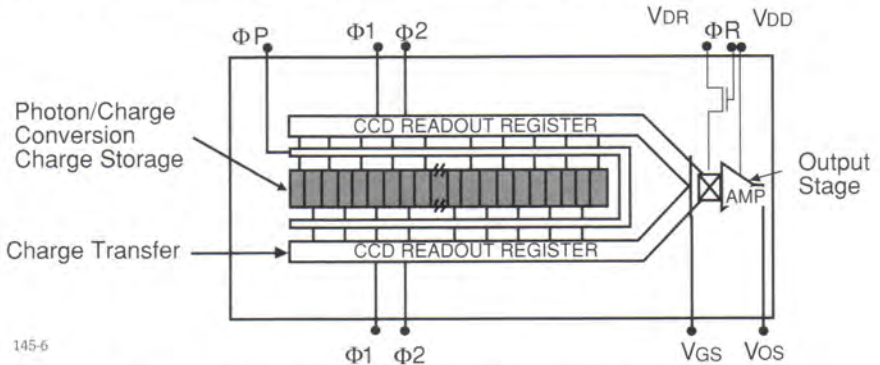
Figure 4 - Theoretical functional block diagram of a linear CCD.

We shall now explain how each of these steps is carried out, through a description of a CCD image sensor which uses an n-MOS buried-channel design with two levels of polysilicon gates, a process adopted by Thomson-CSF for its excellent performance characteristics (detailed in table I).

I.2. LIGHT-TO-CHARGE CONVERSION AND CHARGE STORAGE

The input of a CCD image sensor consists of an array of photosensitive elements, or pixels, which carry out the light-to-charge conversion. These can be photodiodes or photoMOS elements (see figure 5) disposed either along a single line or in a two-dimensional matrix.

When a photon enters in the silicon, an electron-hole pair is generated. The electron is collected in a depleted zone created by means of a diode or a MOS structure, while the hole is re-combined in the silicon substrate.

I.2.1. - Photoelement Structures : Photodiode and PhotoMOS

In the photodiode structure, an N^+ region is implanted in the P-type substrate so as to form a P-N diode. This diode can be reverse biased by an overlying polysilicon gate to create a space-charge zone in which photoelectrons are separated from holes ; photoelectrons are then accumulated in the N^+ zone.

In the photoMOS structure, the space-charge region is induced by a polysilicon gate overlying a thin oxide layer. After electron-hole separation, charge accumulation occurs in the inversion layer.

145-7
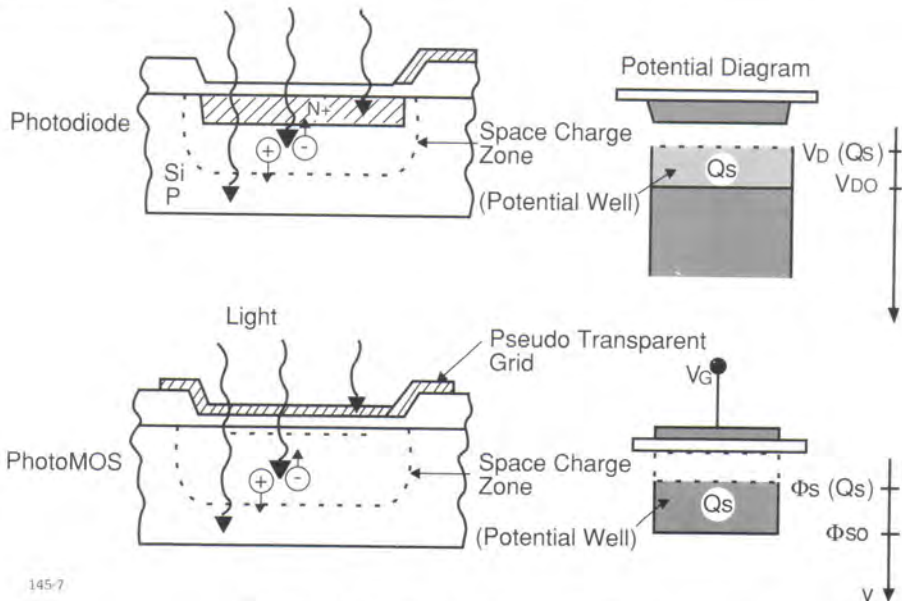
Figure 5 - Photodetection using silicon

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The photoMOS structure can be used both to store photoelectrons and to transfer charges, depending on the clock voltages applied to the different gates. The voltage configuration on successive gates creates localized potential gradients in the substrate, forming potential wells.

Figure 5 shows the generally-used symbolic representation of a potential well, which is the one-dimensional potential diagram of the region where charges are stored. The arrow points along the direction of increasing potential. The hatched area shows the presence of charges in the potential well.

I.2.2. - Buried-Channel and Surface-Channel MOS Structures

As can be seen from Figure 6, a buried-channel MOS structure has a thin doped layer (usually N-type), close to the oxide interface, and oppositely doped with respect to the substrate (usually P-type). As a result, the potential gradient beneath a biased gate reaches a maximum value within the N layer and falls down to 0V in the P-type substrate. The lowest energy state (bottom of the potential well) for a photoelectron will therefore be inside the N zone, and hence buried beneath the surface of the substrate.
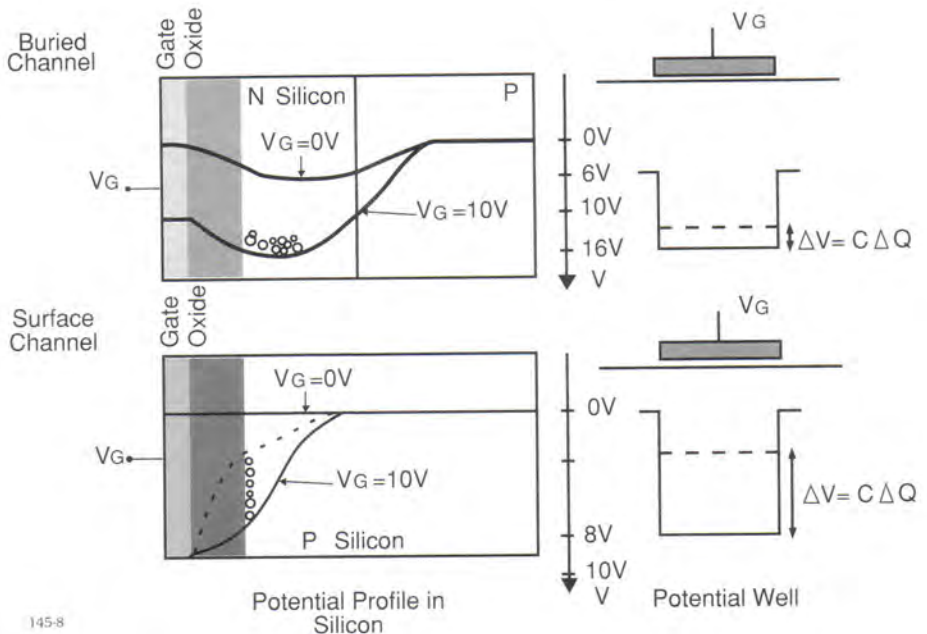
Figure 6 - Buried and surface channel structures.

A surface-channel MOS structure, in contrast, has a uniformly doped substrate. Therefore, when the gate is biased, a depletion region is formed beneath the oxide layer, with the lowest energy state for a photoelectron at the oxide-substrate interface. This means that the photocharges are exposed to the silicon-dielectric surface states, which introduce noise and decrease charge transfer efficiency.

TABLE I - Relative characteristics of buried-channel and surface-channel structures

Characteristic	Buried-channel	Surface-channel
High transfer efficiency	●	
High operating frequency	●	
Low intrinsic noise	●	
Large charge handling capability (for a given clock voltage)		●

Thomson-CSF devices are fabricated in buried channel technology, in order to obtain all the above mentioned benefits.

I.3 - CHARGE TRANSFER OPERATION

Charge transfer is the operation which displaces packets of photocharges along the array of elements to the final output stage. It is characterized by the number of different clocks required to bring the photocharges from one element to its neighbour.

Here, we shall describe two-and four-phase transfer operations. Both are used in Thomson-CSF image sensors and have their own sets of characteristics.

I.3.1 - Two-Phase Operation

Figure 7 shows the electrode succession and resulting potential wells for two neighbouring stages with three different clock configurations, at times A, B and C. Note that there are two levels of gate, denoted Si1 and Si2 . Adjacent two-level gates (Si1 and Si2) are interconnected in alternate pairs to respective drive clocks, $\Phi 1$ and $\Phi 2$, which induce the appropriate sequence of potential wells in the substrate. An N-zone is located beneath the Si2 gate in order to modify the potential distribution, so as to achieve a built-in unidirectional transfer structure.
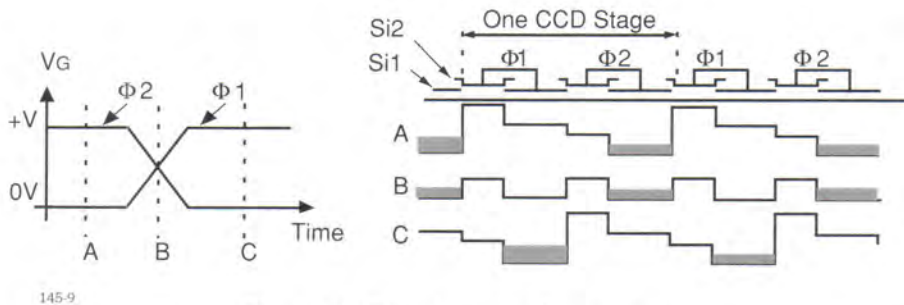

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Figure 7 - Two-phase transfer operation

If at time A, clock $\Phi 1$ (say) is at 0 V and clock $\Phi 2$ at a positive voltage +V, the potential

well profile will be as shown on line A. The photocharges (shown in hatched lines) will settle beneath the Si1 gate driven by $\Phi2$.

The transfer is initiated by raising $\Phi1$ to $+V/2$ and simultaneously decreasing $\Phi2$ to $+V/2$ (time B), creating the potential well profile shown on line B.

Next, $\Phi1$ is set to $+V$ and $\Phi2$ to 0 V (line C) ; with the collapse of the potential well beneath $\Phi2$, the photocharges move to the potential well now formed under the $\Phi1$ clock.

This cycle is then iterated, starting at line A, with the charges shifted along one half stage at each new change in the $\Phi1$, $\Phi2$ clock configuration.

I.3.2. - Four-Phase Operation

As with a two-phase sensor, the four phase structure uses alternate Si1 and Si2 gates. In this case, the gates are clocked independently. No implanted zones are used, since unidirectional flow is achieved by biasing each gate separately ; the transfer direction is therefore determined solely by the clock timing sequence. Figure 8 shows the four successive
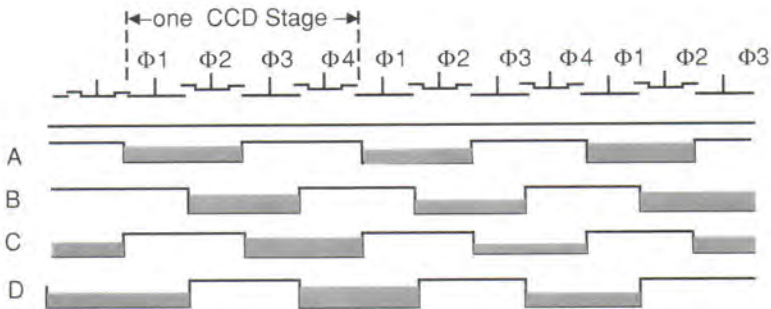
145-10

Figure 8 - Four phase transfer operation
potential well configurations (A, B, C, D) during transfer from one pixel to the next.

At time A, two adjacent gates (in this example clocked by $\Phi1$ and $\Phi2$) are biased to the same voltage $+V$, while the next two gates along, clocked by $\Phi3$ and $\Phi4$, are kept at 0 V, so forming a barrier to isolate the potential wells.
In the first transfer sequence (time B) $\Phi3$ is clocked to $+V$ and $\Phi1$ is set to 0 V while $\Phi2$ and $\Phi4$ remain as before ; the photocharges are thus shifted along one electrode space, since those stored under $\Phi1$ and $\Phi2$ are drawn to the new well under $\Phi2$ and $\Phi3$.
During the next sequence (time C), $\Phi4$ is raised to $+V$ and $\Phi2$ is set to 0 V, again shifting the photocharges, this time to the well under the $\Phi3$ and $\Phi4$ gates.
Iteration of this sequence displaces the photocharges unidirectionally from one element to the next. As one stage is formed by four adjacent gates, the cycle is completed in four elementary transfers.
The main differences between two and four-phase sensor characteristics are given in the following table.

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TABLE II - Relative advantages of two and four-phase sensors.

Characteristics	Two-phase	Four-phase	Comment
High charge handling capacity		●	
High dynamic range		●	
High clocking frequency	●		Currently up to 20 MHz
Drive circuit simplicity	●		Sequencer IC available for four-phase sensors
Bidirectional transfer capability		●	

1.4 - READOUT STAGE

As the charges arrive at the readout stage, they are converted to a proportional voltage level. This conversion is carried out by a readout diode, adjacent to an output gate, V_{GS} (DC bias). After readout, charges are drained away in a reset diode via a MOS transistor (figure 9).

The readout sequence is divided in three successive steps :

(The $\Phi 3$ and $\Phi 4$ clocks shown correspond to the last stage of the transfer sequence. In the example, the transfer stages are of the 4 -phase type).

a) *Diode reset* - The reset clock (ΦR) is set high, switching on the reset MOS transistor, and thus the readout diode is set to reset diode voltage (V_{DR}). At this stage, charges in the readout diode (corresponding to the preceding video signal) flow through the reset MOS transistor and are drained by the reset diode.
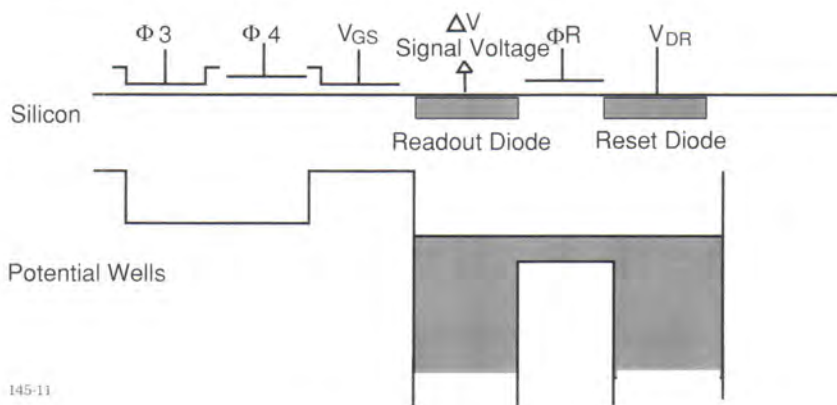
145-11

Figure 9a - Diode reset

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b) *Floating diode* - ΦR returns to its low level. The readout diode is then isolated at a high impedance state. However, parasitic coupling by the reset MOS causes the readout diode voltage level to decrease somewhat during high-to-low transition of ΦR
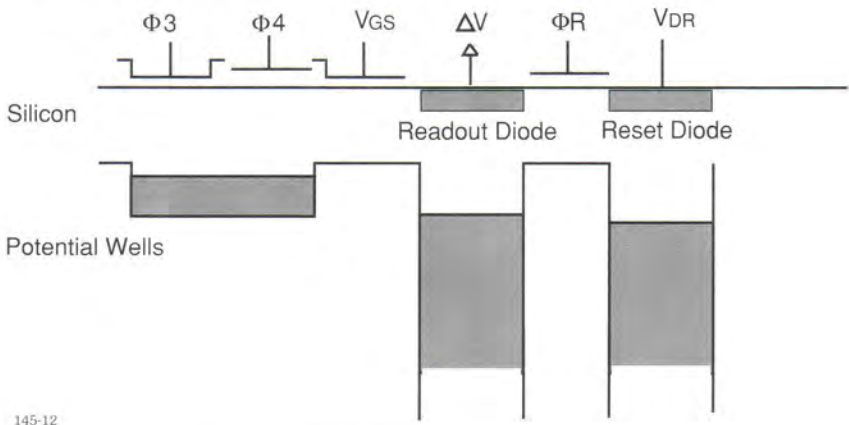
Figure 9b - Floating Diode

c) *Charge sensing* - Here, the last-stage transfer clock returns to 0 V in order to send charges to the floating diode (V_{GS} is permanently biased to provide the necessary potential gradient). The diode voltage then decreases by an amount :

$$\Delta V \text{ signal} = \frac{\Delta Q \text{ signal}}{C_L}$$

where C_L is the reverse-biased diode's capacitance and ΔV signal is the voltage difference before and after the arrival of charge, namely the induced signal voltage.
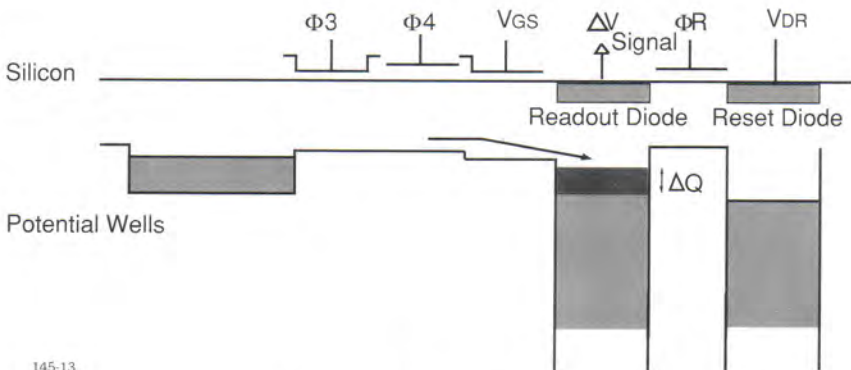
Figure 9c - Charge sensing

This voltage is fed to an amplifier (which may incorporate a sample-and-hold circuit) before reaching the sensor output (see figure 10).

$$V_{OS} = G\Delta V \text{ Signal} = \frac{G}{C_L} \times \Delta Q \text{ Signal}$$

G= Amplifier Gain

145-14
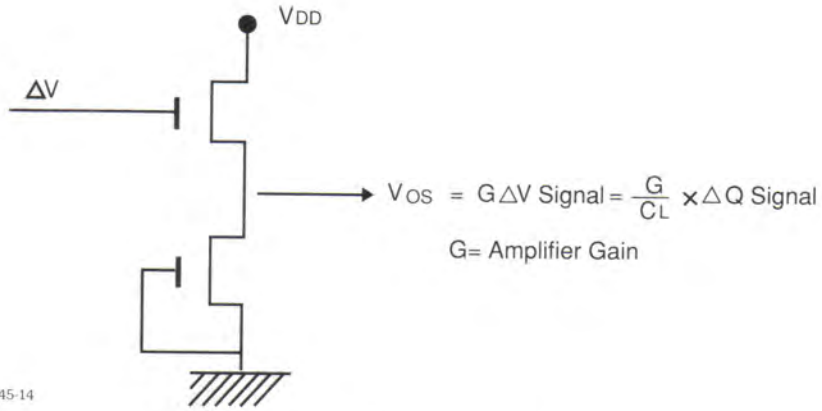
Figure 10a - Output amplifier

Φ4

ΦR

Reset Level

Floating Diode

Vos

Video Signal
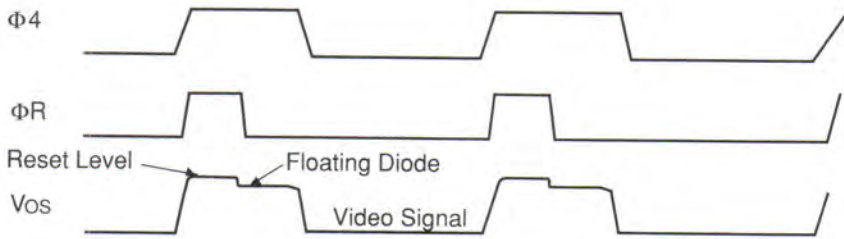
Figure 10b - Output signal versus ΦT and ΦR

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PART II
ELECTROOPTICAL PERFORMANCE

We shall now look at the main parameters that characterize CCD image sensors.

II.1 - RESPONSIVITY (R)

R is the ratio of useful signal voltage (Vos) to exposure, for a given illumination.

It is a function of two parameters :

- photoelement sensitivity,
- charge-to-voltage conversion.

II.1.1 - Sensitivity (S)

S expresses the number of photocharges generated from a given exposure.

Sensitivity, or quantum efficiency, is defined as the ratio :

$$\frac{\text{no. of collected photocharges}}{\text{no. of incident photons on pixel area}}$$

This parameter depends on :

$$- \text{pixel aperture} = \frac{\text{photosensitive area}}{\text{pixel area}}$$

- photosite structure (mainly whether photoMOS or photodiode).
- substrate structure (mainly the thickness of the optically active layer).

For example, with blue-wavelength illumination, a photoMOS structure is less sensitive than a photodiode structure, all things being equal. But a 100 % aperture photoMOS pixel can have a sensitivity similar to that of a 20 % aperture photodiode pixel.
With charge expressed in Coulombs (Cb) and incident photons measured by their energy in Joules (J), S is given in Cb/J or A/W.

$$\frac{Q}{E} = \frac{I \, \Delta t}{P \, \Delta t} = \frac{I}{P} \qquad \begin{array}{l} Q = \text{Charge} \; ; E = \text{Energy} \\ P = \text{Power} \; ; t = \text{Time} \end{array}$$

For Thomson-CSF CCD image sensors, the aperture ratio depends only on whether or not the elements have a built-in antiblooming device (see Section II.13) :

- sensor without antiblooming : aperture = 100 %
- sensor with antiblooming : aperture ~ 70 %

II.1.2. - Charge-to-voltage conversion

Charge-to-voltage conversion is carried out by the readout diode. If:

Q_L = sensed charge value,

and C_L = sensing capacitance,

The resulting voltage on the diode will be : $V_L = \dfrac{Q_L}{C_L}$

Applying this voltage to the output amplifier of gain G will result in a final video output signal:

$$V_{OS} = GV_L = G \frac{Q_L}{C_L}$$

The output conversion factor is defined as:

$$K = \frac{V_{OS}}{Q_L} = \frac{G}{C_L}$$

K is usually referenced to the electronic charge q and expressed in $\mu V/ e^-$; in this

case : $K = q \dfrac{G}{C_L}$

The output amplifier is made with MOS source followers, and its voltage gain G is typically 0.7.

A typical value of C_L is 0.08 pF, giving a K factor of 1.4 $\mu V/ e^-$.

II.2 - SPECTRAL RESPONSE

Responsivity is a function of the illuminating source wavelength, whose plot gives the spectral response curve (figure 11).

Spectral response depends on the photoelement structure (photodiode or photoMOS) and on the type of silicon substrate used.
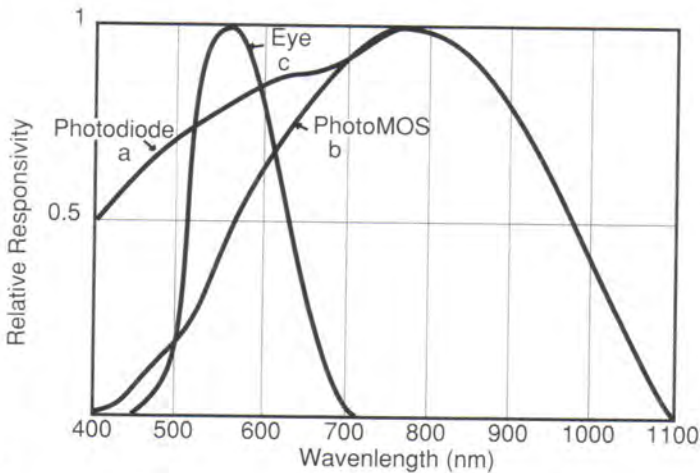
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Figure 11 - Typical spectral responses for:
a) a photodiode
b) a photoMOS
c) the human eye, for reference.

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The relative electrooptical characteristics of both structures are summarized in table III.

TABLE III - Comparison of photoMOS and photodiode elements

Characteristic	Photoelement structure	
	Photodiode	PhotoMOS
Average quantum efficiency η_m in the visible spectrum	60 %	30 %
Spectral response (see figure 11)	Uniform. Higher than photoMOS in the blue region ($\eta = 50$ % at 450 nm)	Irregular and poor in the blue region ($\eta = 20$ % at 450 nm)
Storage capacity	Poor	Good
Image lag	Yes (can be reduced by bias charge)	No

As can be seen from the spectral response curves (figure 11), the difference in the average quantum efficiency of the two photoelement structures is significant for wavelengths below 700 nm. Note that both structures have a good response in the near- infrared spectrum up to 1100 nm.

The spectral response of the photoMOS is lower towards the blue region owing to the fact that the photons have to cross the poly Si electrodes before entering the photosensitive silicon, and their mean free path decreases with wavelength. It is possible to overcome this phenomenon through device thinning and backside illumination.

The storage capacity of the photodiode is relatively low owing to the wide extension of the space charge.

II.3 - PHOTORESPONSE NON-UNIFORMITY (PRNU)

Local variations in the different layer thicknesses or in the geometry of the pixels generate modifications in quantum efficiency along the photosensitive area. As a result, for a uniform illumination, charge signals will be somewhat different from one pixel to another and there is thus what is termed photoresponse non-uniformity.

PRNU depends on light wavelength and substrate structure ; in particular, near infrared light penetrates deeper in silicon and exaggerates the effects of substrate non-uniformities.

II.4. - SATURATION VOLTAGE (VSAT)

V_{SAT} is the maximum output signal voltage the sensor can deliver. It depends on the same conversion parameters as responsivity. This maximum voltage is limited by either one of the following factors :

- storage capability

The maximum quantity of photocharge that can be stored in a photoelement is influenced by many factors which are widely inter-dependent. The photoelement storage capacity will increase with :

- increase in photoelement or transport register dimensions.
- use of four-phase design as opposed to two-phase
- use of surface channel technology as opposed to buried channel
- increase in clock voltages
- use of a photoMOS structure as opposed to a photodiode.

- output diode capacitance, determined by output diode area.
- reset voltage. A low reset voltage limits the charge handling capability of the output diode.
- output amplifier clipping.

II.5 - LINEARITY

With CCD image sensors, the output signal is directly proportional to exposure (Gamma factor = 1). But this linearity can be limited by secondary effects :

- readout capacitance non-linearity (part of which is due to the voltage-dependent depletion capacitance),
- output amplifier non-linearity, due to the bulk effect on MOS transistors.

Secondary effects result in non linearity values of typically less than 1 %. At very low signal values, non-linearity may increase as a consequence of photosite lag (see Section II.12).

When approaching saturation, linearity deteriorates rapidly.

II.6 - CHARGE TRANSFER EFFICIENCY (CTE)

CTE measures the percentage of charges transferred from one stage to the next .

CTE decreases when drive clock frequency increases, but the efficiency remains fairly good above 20 MHz with buried-channel transfer.

It also decreases when gate length increases, since the maximum possible clock frequency is inversely proportional to gate length. This means that a given CTE is a trade-off between the maximum operating frequency and gate length (which partially determines the pixel pitch).

The percentage of well-transferred charge after N stages is given by :

$(CTE)^N = (1-\varepsilon)^N \sim 1 - N\varepsilon$

where ε is the charge transfer inefficiency for one stage.
Since CTE contributes to the Contrast Transfer Function limitation, the resolution on the last pixels will be lower than on the first ones.

II.7 - DARK SIGNAL (VDs)

VDS is generated in the silicon by thermal agitations which energize some electrons into the conduction band ; these electrons are trapped in the potential wells and assimilated with the signal. This thermal charge is proportional to time and is a strong function of temperature : dark signal doubles for every 8 to 10 °C temperature rise (above -25 °C). It is thus important to minimize the sensor's operating temperature, and bear in mind that the more thermal charge there is, the less room there remains for signal charges.

Thermal charge is created not only in the photoelements but also in the transfer stages. In particular, there will be a steady and noticeable rise in the thermal charge content between reading out the first and the last pixels if the readout time is too long.

II.8 - NOISE SOURCES

Typical values of the different noise sources are given in table IV.

II.8.1 - Photonic Noise

This noise is a consequence of the corpuscular nature of light, which gives rise to shot noise, whose value is equal to $\sqrt{Ns}$ where Ns is the number of electrons in a pixel. Photonic noise constitutes the major noise source at low illumination levels.

II.8.2 - Temporal Noise :

Defined as the fluctuation in time of a given pixel signal in darkness, temporal noise is generally quantified by its r.m.s. value. (r.m.s. = root mean squared).

The main contributions to temporal noise are :

- *reset noise*, introduced when charging the diode to its reference potential.

   Its r.m.s. value is given by :

$$\left(\frac{kT}{C_L}\right)^{1/2} \text{ in volts, or } \frac{1}{q} (kTC_L)^{1/2} \text{r.m.s. electrons}$$

   where k = Boltzmann constant
   $\quad\quad\quad$ T = Absolute temperature
   $\quad\quad\quad$ C_L = Readout capacitance
   $\quad\quad\quad$ q = Electron charge

   For example, at room temperature (300 K), the reset noise (in r.m.s. electrons) is about $400 (C_L)^{1/2}$, with C_L in picofarads.

- *amplifier noise*, including Johnson (thermal) noise and 1/f MOS transistor noise.

Other contributions result from :

- *dark signal level*. Dark current is a random process similar to photon emission. Its r.m.s.

noise contribution is given by $(N_0)^{1/2}$ where N_0 is the number of electrons corresponding to the dark current.

- *transfer noise*, which is related to transfer efficiency and given by $\sqrt{\varepsilon.N.N_s}$ where :

N = Number of stages
ε = Charge transfer inefficiency per stage (see Section II.6)
N_s = Charge transferred

II.8.3 - Fixed pattern noise :

Under this term are gathered all time-independent noise contributions introduced by spatial fluctuations in the video signal. It has two origins:

- The first comes from dark signal non-uniformities due to inhomogeneities in the substrate. One of the major reasons for such spikes is local crystal defects. This highlights the importance of using high-quality substrates and optimized annealing processes to minimize this parameter.

This component of dark signal non-uniformity (DSNU) has the same variation law as the average dark signal, and is the main limitation as regards detectivity performance.

- The second source includes non uniformities that are independent of temperature and illumination, as well as time. The origin can be spurious transients introduced by clocks, interferences from power supplies, or other external sources.

II.8.4 - Noise introduced by a bias charge :

If an electrical bias charge is added (as recommended for certain devices to improve photodiode to register transfer efficiency) it will introduce an input noise of same nature as reset noise, given by : $400\,(C_{IN})^{1/2}$ (C_{IN} input capacitance in pF).

If the bias charge is generated by illumination of the photosite, it will introduce shot noise of same type as photon noise, equal to : $(N_{BIAS})^{1/2}$, where N_{BIAS} is the bias charge in electrons. Typical values of temporal r.m.s. noise contributions for a buried channel device under normal operating conditions are given in Table IV below.

TABLE IV : Typical values of temporal noise

Noise Source		Variation law	Value (r.m.s. electrons)	Conditions
Photon noise		$\sqrt{N_S}$	1000 100	$N_S = 10^6$ (1) $N_S = 10^4$
Reset Noise		$400\sqrt{C_L}$	110	$C_L = 0.08$ pF
Amplifier noise (1/f MOS transistor noise excluded)		$\sqrt{N_{DS}}$	100-200	BW= 1 MHz
Dark current			20	$V_{DS} = 0.5$ mV K= 1.4 µV/e-
Bias Charge	Electrical input	$400\sqrt{C_{IN}}$	120	$C_{IN} = 0.1$ pF
	Introduction in photosites	$\sqrt{N_{BIAS}}$		$N_{BIAS} = 5.10^5$

(1) : typical full well capacity corresponds to $N_s = 1$ to 2×10^6 electrons

II.9 - DYNAMIC RANGE

Dynamic range is defined as the ratio of the saturation voltage to the r.m.s. temporal noise.

This formulation of dynamic range is of practical value only if the DSNU (Dark Signal Non-Uniformity) is lower than the r.m.s. noise, or if, for each pixel, the dark value is subtracted from the signal value.

II.10 - RESOLUTION AND CONTRAST TRANSFER FUNCTION (CTF) :

Spatial resolution characterizes the ability of the photosensor to discriminate between closely spaced details in the scene. It is measured by the response of the photosensor to a pattern of equidistant black-white bar pairs (as used in TV test charts) of increasing spatial frequency.

An upper limit to the correct reproduction of such a pattern is the pixel's spatial frequency, or Nyquist frequency, defined as : $F_N = 1/2 \, d$; where d = pixel pitch

the factor 2 comes from the fact that at least two pixels are necessary to sample a pair of bars correctly.

Starting from 100 % contrast at zero spatial frequency, obtained from the difference between the black and white levels without any pattern, the value of this contrast is progressively reduced as the spatial frequency of the pattern increases. The corresponding contrast curve, where ordinate amplitude is expressed as a percentage of the zero frequency contrast and abscissa represents relative spatial frequencies F/F_N, defines the Contrast Transfer Function (CTF).

Spatial resolution may also be characterized by its modulation transfer function (MTF) obtained as for CTF but using a sinusoidal spatial modulation of the source intensity instead of the black-white stripes.

The factors that affect the more-or-less rapid decrease in CTF as spatial frequency approaches the F_N limit are :

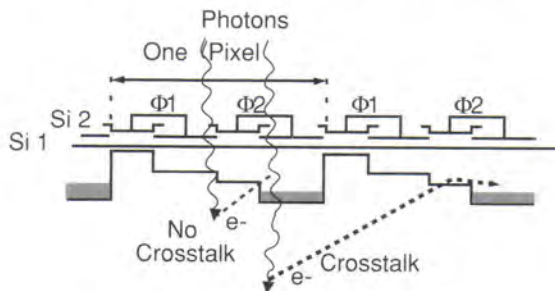- *geometric definition of the photoelement* : pitch and aperture ratio,

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Figure 12 - Crosstalk between pixels

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- *carrier diffusion degradation (crosstalk)* : because of imperfect separation between potential wells, some electrons generated under a pixel will diffuse to the neighbouring ones.This effect will be more pronounced with long wavelength photons, since they are absorbed deeper in the silicon.
This degradation also depends on the type of isolation used between photosites and on substrate structure.

- *Transfer inefficiency* : this factor is minor with buried chanel devices, owing to their high CTE value.

Typical values of CTF at Nyquist Frequency (FN) are 50 % to 70 % when excluding the degradation due to the lens.

II.11 - MAXIMUM OUTPUT DATA RATE

The output frequency is limited either by the amplifier bandwidth, or by the speed performance of the internal logic circuits.

Transfer registers are not generally a limitation to the maximum output frequency.

II.12 - LAG

This is the image trailing effect caused by residual photocharges left in a photoelement after a transfer operation.

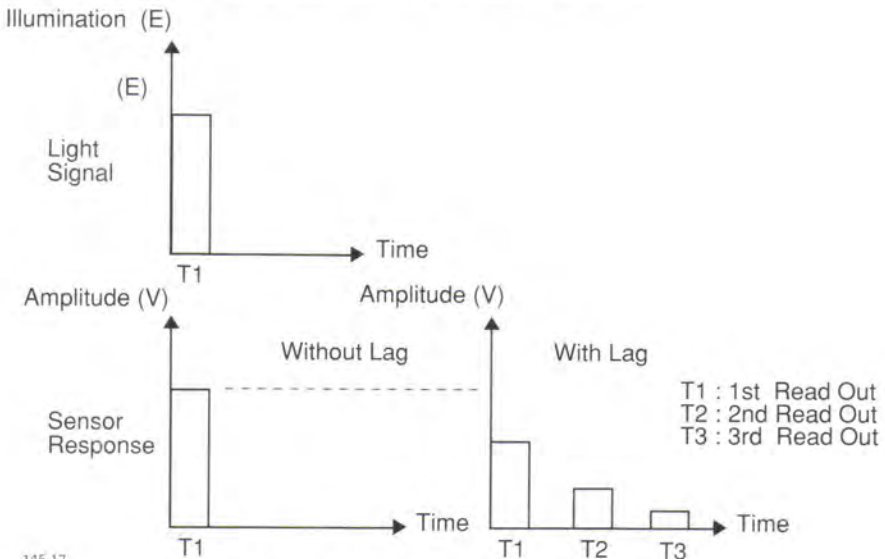Lag is only noticeable with sensors having photodiode elements.

Figure 13 - Lag due to a light pulse

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With a diode, the associated potential well contains an inifinite number of electrons. In the continuous dark mode, the diode settles to a thermodynamic equilibrium which fixes the diode potential at a level (L0) that is greater than the storage gate potential (L1) (see figure 14).

Now, a given exposure will generate a certain amount of charge that can be broken down as Q1 + Q2. Q1 is the quantity of charge that is transferred rapidly into the readout register potential well (this is the equivalent to a transfer into a MOS capacitor). Q2, on the other hand, will be transferred during the return to thermodynamic equilibrium.

The shorter is the open period of the transfer gate, the longer is the return to thermodynamic equilibrium, and hence the greater is the lag effect.
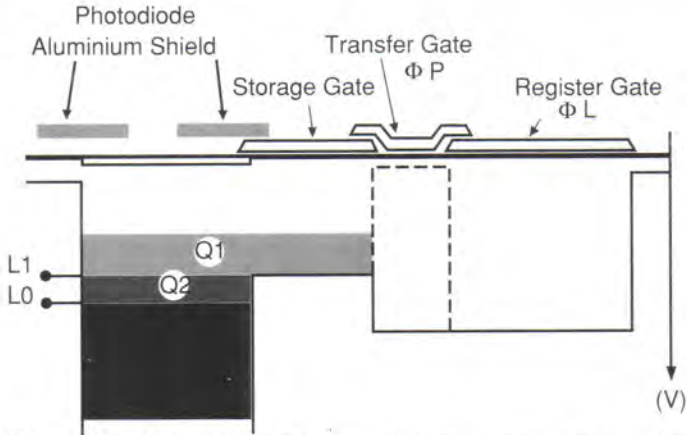
Figure 14 - Linear CCD photosensitive zone to register transfer.

With a photoMOS, the potential well contains a finite number of electrons (generated either by incident photons or the dark current) which can all be transferred into the neighboring potential well. Good charge transfer is characterized by a high CTE, which depends on the time taken to transfer the photocharges from one well to the other. Lag charge decreases as transfer time ($T \Phi P$) increases.

Lag can be reduced by the introduction of a "fat zero" (electrical or optical bias charge) .

II.13- OVERILLUMINATION RESISTANCE (antiblooming)

This is the ability of a saturated photoelement to prevent excess photocharges from spilling over to neighbouring ones (blooming phenomenon).

Blooming is usually well localized and can arise with scenes containing very strong local illuminations which are not accommodated for by the lens aperture setting and/or the exposure period. The spread of photocharges appears as a white blot or streak on the TV monitor.

There are two major antiblooming structures in use :

a) *Vertical structure (figure 15a)* - A deep diffusion is made to allow extra charges to be drawn towards the substrate, where they can recombine.
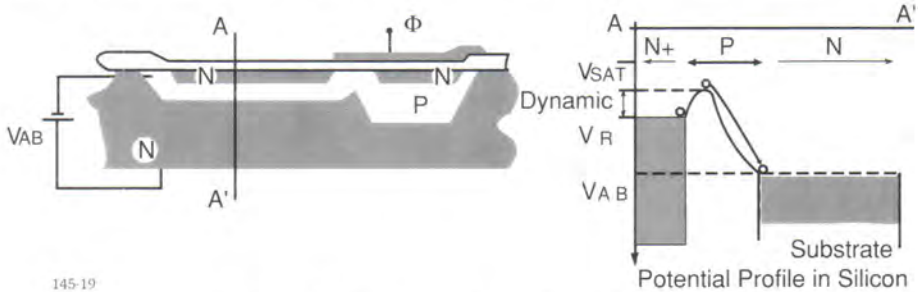
Figure 15 a - Vertical antiblooming structure.

b) *Horizontal structure (figure 15b)* - A diode (antiblooming diode) is implanted at each photosite and is separated from the potential well by a control gate. This gate is biased to adjust the potential barrier between the photocharges and the antiblooming diode to a level lower than the potential well separating two neighbouring wells, so that all excess charge will overflow into the antiblooming diode. The antiblooming control gate bias therefore determines the saturation level.

This solution is adopted by Thomson-CSF because it does not reduce near infrared sensitivity.
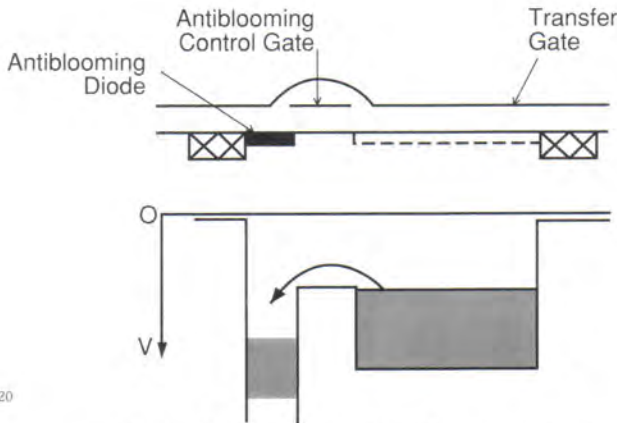
Figure 15 b - Horizontal antiblooming structure.

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PART III
THOMSON-CSF LINEAR CCD IMAGE SENSORS

Linear CCD image sensors contain a single line of photoelements associated to charge transport shift registers and one or several output amplifier(s). They are used either in fixed systems (e.g. for spectroscopy, bar-code readers, metrology), where a single line is analyzed, or in two-dimensional analysis. In the last case, a scanning type system is required to analyze the image as a succession of lines by a relative displacement of the sensor and the scene (e.g. for facsimile, telecinema systems, industrial control, earth observation, etc ...).
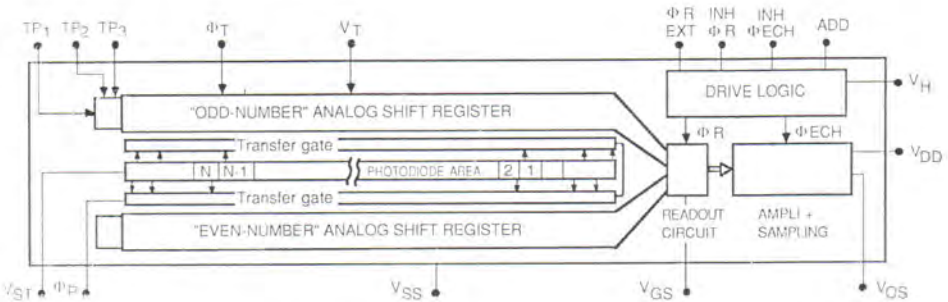

Figure 16 - Typical organization of a Thomson-CSF linear CCD image sensor with on-chip multiplexing.

III.1 - THE PHOTOSENSITIVE ARRAY

Photoelements are made of N photodiodes separated by an insulation barrier. The vertical aperture is defined by an aluminium shield. A MOS capacitor is associated to each photodiode in order to increase its maximum storage ability. The MOS gate reverse biases the diode and creates the potential well to store charges.

III.1.2 - Photoelement-To-Shift-Register Transfer

Alternate elements along the photosensitive array (designated odd and even elements) are associated to respective CCD analog shift registers located on either side - charge transfer from photoelement to shift register is carried out by a transfer gate, which creates a variable potential step between the two. This barrier between the photodiodes and the shift registers is controlled by an external clock signal, the transfer clock (ΦP), which determines the exposure period.

During image exposure (integration period) the photodiodes are isolated from the shift register and biased to accumulate photocharges.

Figure 17 shows a cross-sectional view of the structure connecting a photodiode to its shift register stage. When ΦP is set to 0 V, the storage zone is isolated from the potential well created under the shift register gate, and thus no transfer can take place.

At the end of the integration period, ΦP is clocked to a high voltage such as to induce a potential well for bridging the photoelement and shift register potential wells. Charge is transferred from the photoelement to the shift register if the wells are successively deeper, as shown by the dotted line.
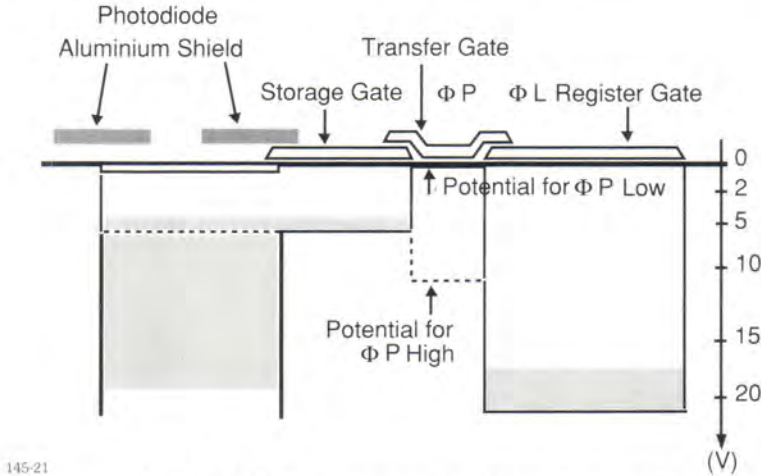

Figure 17 - Gate structure and potential well profile
for photosensitive zone to register transfer.

To satisfy this condition, the shift register has a buried channel structure so that a 12 V bias (say) on the its gate (clocked by ΦT) induces a well depth of around 20 V. The substrate under ΦP has a surface channel structure so that its well depth is smaller for an equal bias voltage. The photoelement is biased at a lower voltage.

III.1.3 - Charge Transport Along Shift Registers

Once the photocharges are emptied from the photodiodes and loaded into the shift registers, the photodiode array is ready to integrate new packets of photocharge while those that have just been loaded are transferred sequentially along the shift registers. This is carried out in accordance with the two-phase transfer principle ; for most devices, one clock is set at a constant and intermediate bias (V_T) limiting the number of transport clocks to one (transport clock ΦT).

On the outer sides of the two shift registers are disposed dummy registers which protect the main registers from spurious charges due to lateral illumination.

III.1.4 - Output Stage.

III.1.4 - Output Stage.

There are two basic sensor architectures, depending on the maximum data output frequency required
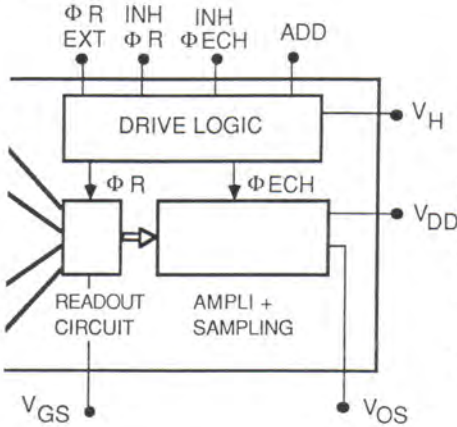

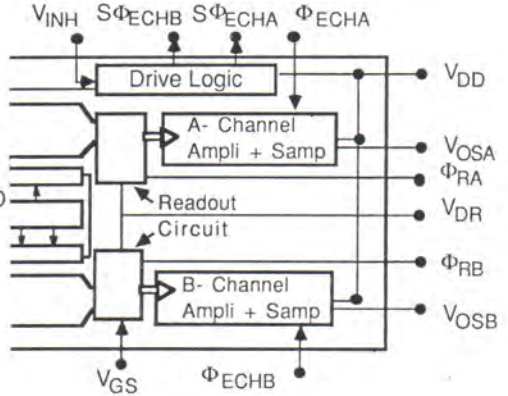**Figure 18a** - Output stage of a medium-frequency sensor (up to 2 MHz data output frequency)

Figure 18b - Output stage of a high-frequency sensor (20 MHz data output frequency and over)

The essential difference in the architecture of medium and high speed sensors is that the former has an internal multiplexing circuit to combine the odd and even element shift registers into a single channel. It this case, the data rate is twice the transport frequency. As on-chip mulitplexing is more difficult to incorporate at frequencies in the 10 MHz range, high speed sensors have separate output stages.

Most linear arrays include an optional sample-and-hold function between the two output amplifier stages.

III.2 - DRIVE SIGNAL CHARACTERISTICS

Figure 19 shows timing diagrams for the Φ and ΦT drive clocks and the resulting output signal in the normal mode (i.e. with all internal clocks used).

The integration period (Ti) is determined by the falling edge of two consecutive ΦP pulses. This is therefore the maximum time allowed to clock out the shift register stages with the ΦT clock. The actual number of stages contained in the register is equal to the number of photoelements, plus some isolation cells and dark reference elements at each end (these are specified in the data sheet).

The dark reference elements are shielded photoelements which reproduce the dark signal voltage of the photodiodes and follow the evolution of this signal with temperature, thereby providing data for dark noise correction. The isolation cells separate the dark references from the photosensitive elements. If the number of reference elements is insufficient for an application, additional references may be obtained by clocking out more shift regis-

ter signals than there are stages between two ΦP pulses, so as to read out the reference (noise) level present on empty stages.
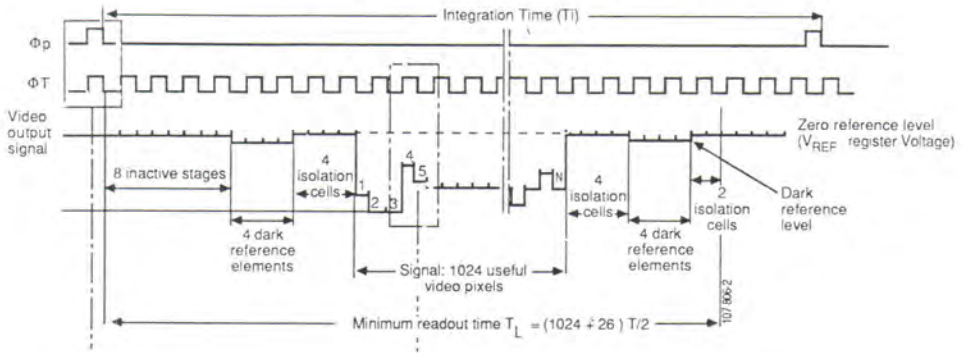
Figure 19 - Timing diagrams for ΦP and ΦT drive clocks and resulting output signal.

III.2.1. - Optional Operating Modes

(Their availability depends on products : please see the sensor's data sheet)

- External reset clock input (ΦR EXT) : gives the possibility of resetting the output stage once for several transport clock periods (ΦT) to group pixels together.

Also, an external ΦR may be used to vary the location and duration of the reset operation, depending on the mode and frequency chosen. In particular, when implementing Correlated Double Sampling, this will give the possibility of adjusting the floating diode and signal durations (see figure 20).
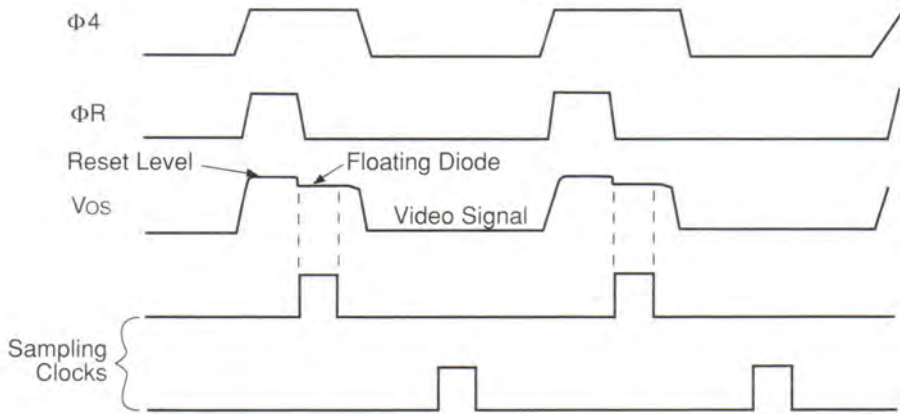
Figure 20 - Timing diagram for correlated double sampling operation

- Internal sample-and-hold clock inhibition : allows delivery of an unsampled output signal (for instance if external sampling is needed).

- Pixel pairing function (ADD) : When enabled, combines pairs of odd and even pixels into a common output signal, so that the sensor effectively acts as if photoelements were halved in number but doubled in size. This is sometimes useful for increasing the sensor's responsivity at the expense of resolution.

To simplify sensor operation, Thomson-CSF produces a series of drive boards which provide all the necessary clock pulses, dc biases and a video output buffer stage. Integration time and transport frequency, as well as all the possible operating mode selections, are controllable by the user.

PART IV
THOMSON-CSF AREA CCD IMAGE SENSORS

Area CCD image sensors contain a two-dimensional matrix of photoelements and can thus be considered as the solid-state analog of a vidicon camera tube. Arrays of up to 300,000 photoelements are commonly available, and monolithic sensors are now used with upwards of 10^6 photoelements in professional fields. They have a very wide range of applications, covering practically every type of TV camera as well as single-field image acquisition systems.

IV.1 - FRAME TRANSFER CCDs

Frame Transfer (FT) is the organization used for all Thomson-CSF area CCD image sensors. Figure 21a shows a TV mode FT sensor, and Figure 21b a single-field mode (full-frame) FT sensor.

• **TV mode FT sensors** : these are characterized by the separation of the element array into two identical areas : an image zone, which receives the optical information, and a masked memory zone, into which the image field is transferred for subsequent readout by the readout shift register. The transfer process along both zones is identical, and can be either two or four-phase.
The memory zone drive clocks (ΦiM) can be driven independently of the image zone drive clocks (ΦiP).

• **Full-frame FT sensors** : these do not have a memory zone, the entire element array forming the image zone. After integration, photocharges are directly transferred line by line in the readout register.
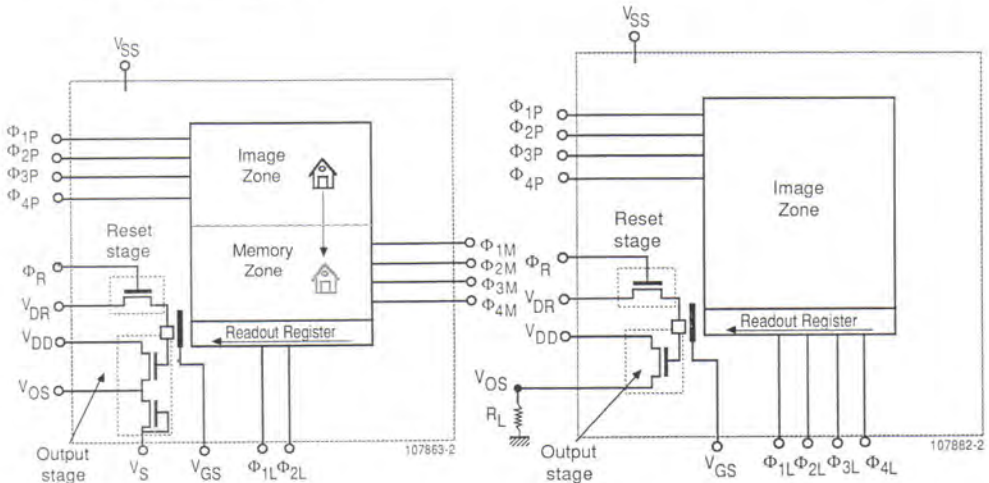

Figure 21a - TV mode FT sensor organization   **Figure 21b -** Full-frame FT sensor organization

IV.2.1 - Image Integration

The image zone is made of a matrix of photoMOS elements. Each column forms a CCD shift register, separated from the others by an insulation wall. The pixels along the shift register are defined purely by gate biases. Shielded columns are added on the edge of the image zone to give a dark reference level for each line.

After transfer of an image into the memory zone, the next image is integrated, i.e. elements in the image zone are biased to accumulate photocharges during the field period imposed by the TV standard (20ms for CCIR and 16ms for RS170).

IV.2.2 - Tranfers From Image Zone to Memory Zone, and from Memory Zone to Readout Register.

Once the integration period is over, charges are transferred from the image zone to the memory zone. This process is carried out during the field blanking period (< 1ms) by activating the ΦiP and ΦiM clocks in phase. The operation has to be as short as possible to reduce the "smearing effect" : incident photons during this transfer time add spurious charges to those which have been accumulated during integration period. After all the charges have been transferred into the memory zone, the image zone is ready to integrate a new field while the memory zone contents are tranferred line by line to the readout shift register at the line blanking frequency.

IV.2.3. - Readout Operation

Each line transferred from the memory zone into the readout register has its charges transported serially to the output stage under the control of separate drive clocks (Φ iL), in either a two or four-phase mode.

Useful pixels are read during the video period, while dummy elements (including dark references) are read during the line blanking period.

The output stage is similar to that of a linear sensor, but is usually without internal sample and hold.

IV.2.4 - Vertical Interlacing

As was shown in the explanation of the transfer operation, charges are accumulated under one or two gates out of the four constituting the photoelement. Photocharges generated outside of the potential well will migrate with a high probability of entering into the nearest well. Thus, the sensor lumps together photocharges from an area extending over four transfer gates (in one dimension) into an area occupied by two (see figure 22).

By inverting the gate biasing on alternate fields (designated odd and even fields), the center of charge collection is shifted to-and-fro by half an element (figure 22). Each CCD element can then be considered as formed of two transfer gates when interlacing on alternate fields. In this way, the effective resolution is increased, even beyond the Nyquist limit imposed by the vertical separation of the elements.

Vertical interlacing should be used selectively. When it is not used, there is the advantage that every field has the same integration structure and gives exactly the same information from one field to the other.
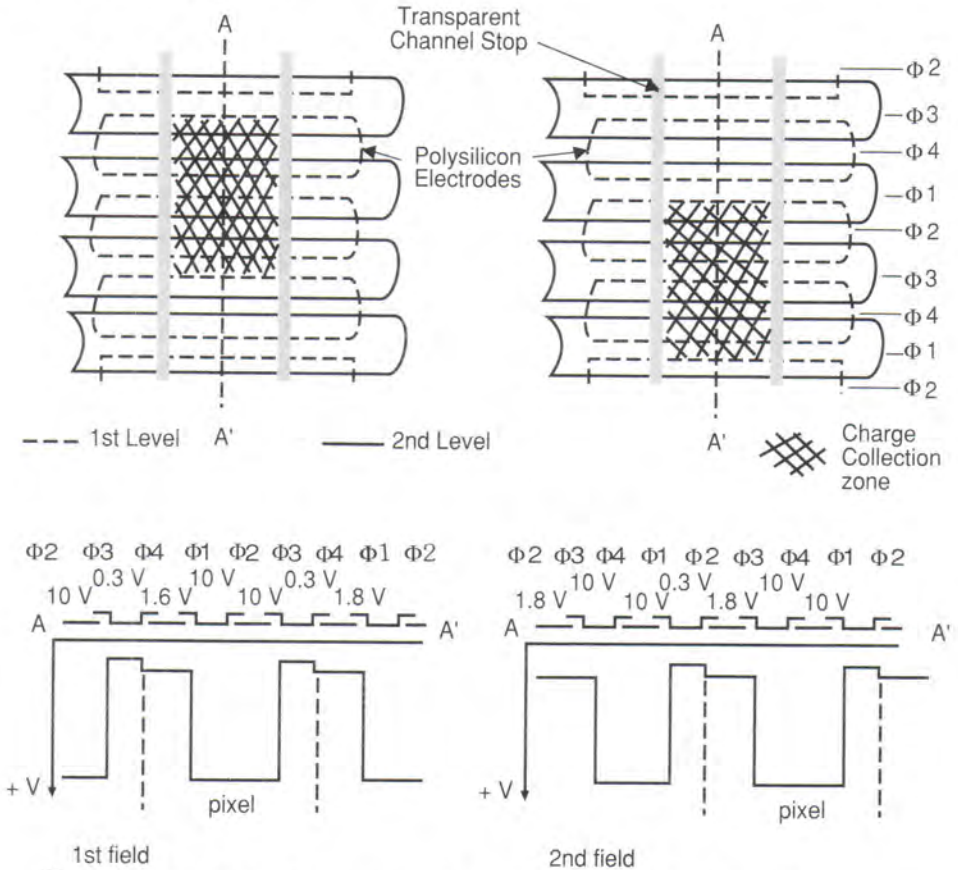
Figure 22 - Charge collection zones and potential well profiles for a CCD element at alternate interlaced fields.

IV.3 - DRIVE CLOCK CHARACTERISTICS

Figure 23 shows an example of the ΦiP, ΦiM and ΦiL clock sequences over two successive interlaced fields for a four-phase sensor.

(Figures 23 through 25 are the timing diagram for the TH 7863 sensor ; however the exact timing sequences will vary from one sensor to another and are given in each sensor's data sheet).
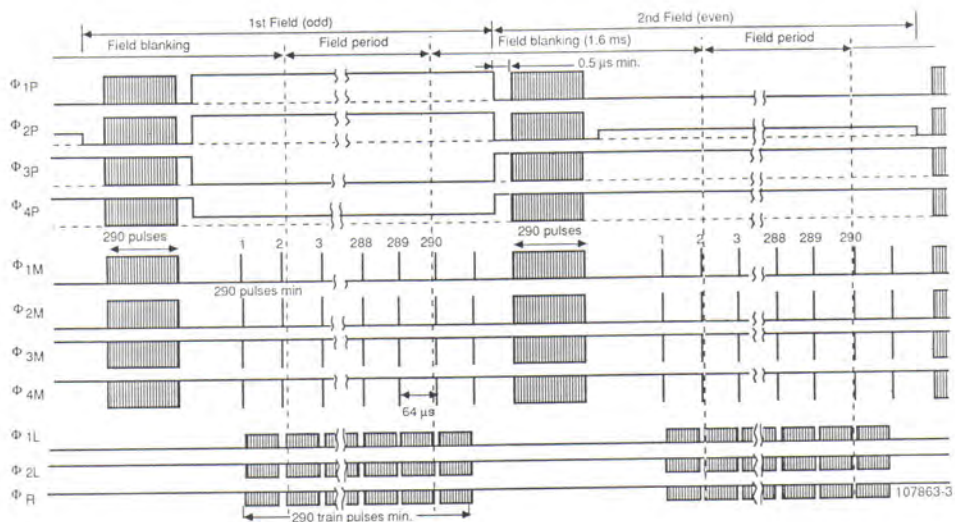
Figure 23 - Frame timing diagram
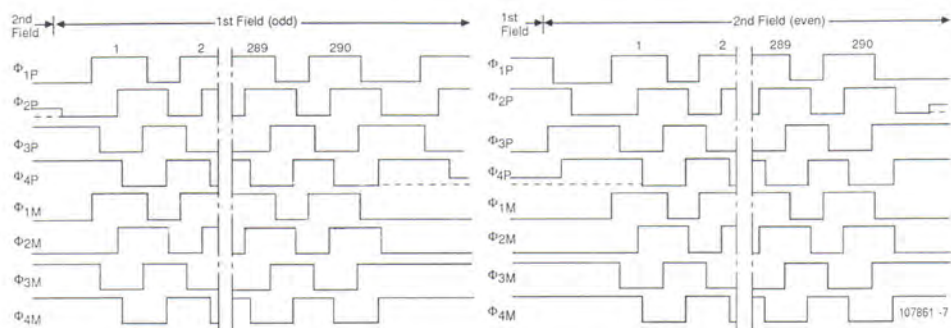
Figure 24 - Vertical transfers during field blanking

Figures 23 and 24 gives relative positions and delays of image and memory zone clocks. Note that during field blanking, i.e. during transfer from image to memory zone, image and memory clocks are identical.

During field integration, the ΦiP clocks are frozen while ΦiM clocks transfer successive lines into the readout shift register. The transfer frequency is the same as the line frequency of the TV standard.

During the line transfer interval, the output shift register is clocked at a readout frequency (FL) chosen to be at least sufficient to feed all the charges into the readout stage before the next line arrives. The relationships between the ΦiM and ΦiL clocks, together with the reset clock (ΦR) and resulting video signal are shown in Figure 25.

For a full-frame image sensor, operation begins with a "cleaning" period, which consists in transferring and eliminating all charges present in the image zone. Once emptied, each pixel can accumulate charges in proportion to incident light during the integration (exposure) period.

After the integration period no luminous event must reach the image zone in order to prevent smearing effects during the readout period.

Once the image is integrated, the photocharges are transferred directly into the readout shift register by the ΦiP clocks, and thereafter to the output stage, as with other sensors.
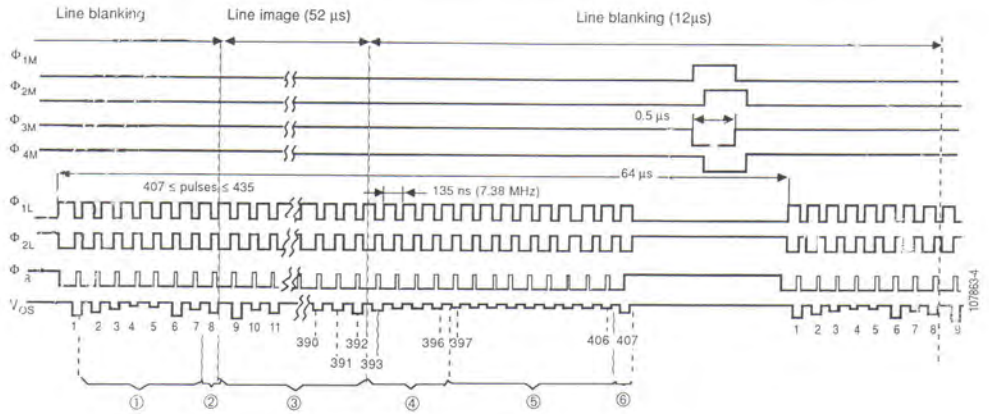

Figure 25 - Line timing diagram

PART V
CCD IMAGE SENSOR PERFORMANCE
DEFINITIONS AND MEASUREMENT PRINCIPLES

V.1. - ELECTRICAL PERFORMANCE

V.1.1 - Clock Capacitance :

The capacitance present between each clock input pin and V_{SS}, measured with a BOON-TON Capacitance Bridge at :

$$V_{DC} = 10 \text{ volts} \quad ; \quad V_{AC} = 1 \text{ volt p.p.} \quad ; \quad F = 1 \text{ MHz}$$

All other pins are connected to V_{SS}.

Clock capacitance has two components : one fixed and due to overlapping gates (C_1), the second a MOS capacitance (C_{OX}) associated with a variable part due to depletion capacitance (C_D). As C_D is not taken in account in measurements, the real capacitance in operation will be substantially lower than the measured one.

V.1.2 - Power Dissipation :

The power consumption of the output amplifier (I_{DD} x V_{DD}) and of the internal logic (I_H x V_H), if incorporated on the chip.

The measurement is made in a static mode, under the following conditions

$$V_{SS} = OV$$
For linear arrays : V_{DD} or V_H at max. value
For arrea arrays : $V_{DD} = 15$ V

All other pins are not connected.

V.1.3 - Peak Current Sink on Drive Clocks :

This current is strongly dependent on clock rise and fall times. The minimum time values are measured with a current probe. Operation with rise and fall times below the minimum value increases the clock current and can damage the device.

V.1.4 - DC Output Level and Output Impedance :

- *DC output level* : The voltage measured at the amplifier output when the reset clock is set to its high state. The reset level of the video signal (V_{OS}) is therefore equal to the DC output level.

- *Output impedance* : This is measured through a capacitor, under typical amplifier biasing, by applying a 100 mV r.m.s./100 kHz sinusoidal signal on the output pin (V_{OS}).

V.1.5 - Charge Transfer Efficiency (CTE) :

Here, the value actually measured is $N.\varepsilon$, where N is the number of stages in the line or column and ε is the transfer inefficiency. As shown in Section II.6, $(CTE)^N \sim 1 - N.\varepsilon$.

In the first step, a uniform quantity of charge is loaded in each of the N stages of the register (or column). Then, $N+1$ transfers are applied ; the $N+1^{st}$ signal represents the total remaining charge. $N.\varepsilon$ is the ratio between the $N+1^{st}$ signal and the average value of the N preceding ones.

Note that on multiplexed linear arrays, the $N+1^{st}$ signal characterizes the odd register with $N/2$ transfers and $N+2^{nd}$ signal characterizes the even register with $N/2$ transfers.

V.1.6 - Maximum Data Output Frequency :

Maximum number of pixel signals per second delivered at the video output (in MHz or pixels/second).

At the minimum guaranteed value of this parameter , the video output signal can be sampled under good conditions.

However, the output rate can be increased if narrow sampling is used. It can be increased even more if a degradation of certain performance characteristics is acceptable.

V.2 - ELECTROOPTICAL PERFORMANCE

V.2.1 - General Measurement Conditions

- Window cleanliness is checked before measurement.

If necessary, lightly wipe the surface with a cotton swab dipped in alcohol ; rince off with deionized water and dry, (preferably with dry N_2 or air) .

- Package temperature T_p is 25 °C . (T_p = 50 °C for dark signal measurements on area arrays).
- Light source is a tungsten filament lamp at 2854 K color temperature with IR cutoff filter.
For linear arrays, the filter is of the Schott KG1 type (2 mm thick) with or without adjunction of a BG38 filter (2 mm thick).
For area arrays, a BG38 filter (2 mm thick) is used .
Illumination is measured at the surface of the device with a silicon detector.

- Numerical aperture of the light source : F/3.5

- All input biases and clocks are at their typical values as specified in the data sheet. If adjustment is required for one bias, it is done before any measurement.

- Output load. The output pin is loaded by an emitter follower whose input capacitance is less than 5 pF. Unless otherwise specified, no load resistor R_L needs to be inserted directly at the video output.

V.2.2 - Unit conversions

V.2.2.1 - Electrophotonic Units.

The tables below give the conversion between various electrophotonic units. Note that the lux is purely a visual unit of illumination which has no significance outside the eye's spectral range. Therefore, all electrooptical parameters involving units of illumination or exposure are quoted in terms of energetic units - respectively W/m^2 or J/m^2.

Exposure = Illumination x Exposure time

$$J/m^2 = W/m^2 \times s$$

TABLE V - Unit conversions

Illumination : energetic/visual unit correspondance.

Unit		Illumination Condition
Energetic (mW/cm²)	Visual (lux)	
10	20	2854 K color temp
5	20	2854 K + BG38

Exposure : energetic/visual unit correspondance

Unit	
Energetic	Visual
J/m^2	Lux.s

Note that responsivity in $V/\mu J/cm^2$ is independent of integration time.

V.2.2.2 - Useful Formulas

- Relationship between number of electrons and readout voltage

$$V_{OS} = q. Ne^- \frac{G}{C_L}$$

Where V_{OS} = Readout voltage (volts)

           q = Electron charge (1.6×10^{-19} Coulomb)

           Ne^- = Number of electrons per pixel

           G = Amplifier gain

           C_L = Readout diode capacitance (Farads)

- Relationship between number of electrons and output current on VDR :

$$I = \frac{q\ Ne^-\ L\ P}{T_i}$$

where : I = Ouput current (read on VDR) (Ampere)
q = Electron charge (Coulomb)
Ne^- = Number of electrons per pixel
L = Number of lines in one field (for linear arrays, $L = 1$)
P = Number of pixels in one line
T_i = Integration time (second)

- Relationship between quantum efficiciency and responsivity :

$$R = \eta\ K\ A\frac{\lambda}{hc}$$

where : R = Responsivity $(V/J/m^2)$

η = Quantum efficiency at wavelength λ

$K = q\ \dfrac{G}{C_L}$: output conversion factor (V/e^-)

A = Pixel area (m^2)
l = Wavelength (m)
h = Planck's constant $(hc = 1.92\ 10^{-25}\ N)$
c = velocity of light

V.2.3 - Saturation Voltage and Exposure

V.2.3.1 - Linear arrays :

Saturation voltage (VSAT) is the maximum output voltage obtained when increasing exposure.

The corresponding light level is the saturation exposure (ESAT)

The saturation level depends on :

- photoelement or shift-register storage capacity
- output capacitance

VSAT is measured by increasing the exposure level up to the point where the output voltage no longer increases and spurious signals begin to appear in the dummy elements (those elements outside of the photosensitive area).

V.2.3.2 - Area arrays

VSAT is the maximum output voltage for which no image degradation occurs (CTF decrease, non linearity, ...)

In measurements, an exposure giving V$_{SAT}$ min (as specified in the data sheet) is applied to the device. CTF and local defects are then checked in order to guarantee the image quality up to that level.

V.2.4. - Responsivity (R) and Spectral Response.

- Responsivity is the ratio of output voltage (V) to corresponding exposure ($\mu J/cm^2$). It is measured at V$_{SAT}$ /2 or V$_{SAT}$ min./2, under specified exposure conditions.

- For spectral response, the definition is the same, but the measurement is made after interposition of a narrow bandwidth optical filter (typically 5 nm).

V.2.5 - Photo Response Non Uniformity (PRNU)

Overall PRNU is the peak-to-peak difference in response between the most and least sensitive elements with respect to the average response, under a uniform exposure giving an output level of V$_{SAT}$ /2.

Low frequency PRNU (or PRNU without localized singular pixels) is measured under the same conditions, but with spikes (measured with respect to neighbouring pixels) excluded.

For area arrays, only low frequency PRNU is specified in the performance characteristic table. Nevertheless, high amplitude spikes are taken in account by image quality grade specifications.

V.2.6 - Dark signal (V$_{DS}$) and Dark Signal Non-Uniformity (DSNU)

Average dark signal is the average video signal in the absence of any illumination on the device, measured under specified temperature, integration and readout times.

Dark signal non-uniformity is measured under the same conditions as low frequency PRNU, but without any illumination and under the same conditions as specified for dark signal.

For area arrays, linear non-uniformity due to memory zone readout is excluded from the measurement ; in fact, the last video line stays in the device for a longer time than the first one (the difference is the readout time). This contribution to DSNU is suppressed by external clamping on dark reference of each line.

V.2.7 - RMS noise (V$_N$) and Dynamic Range (DR)

RMS noise is the rms value of the total temporal fluctuation of a given pixel without illumination. The peak-to-peak value is about six times higher. Bandwidth is limited to the minimum value of maximum output data rate. Dynamic Range is the ratio of saturation voltage to rms noise.

V.2.8 - Contrast Transfer Function (CTF) and Resolution :

CTF is evaluated by imaging a test chart formed of equidistant black and white stripes of a

given spatial frequency under specified illumination conditions and with an average output of $V_{SAT}/2$.

Because of the CCD array's discrete structure, and its consequent aliasing (or moiré) effect, CTF can only be measured up to the Nyquist spatial frequency (F_N), and the measurement is made with maximum phase between the chart and the pixels. Nevertheless, thanks to interlacing on area arrays, aliasing in the vertical direction is largely reduced and the actual resolution is increased ; resolution inTV lines is then defined as the maximum number of lines which can be resolved by the eye along the picture height on a monitor.

V.2.9 - Antiblooming Efficiency

Antiblooming efficiency measures the ability of the device to resist to overillumination.

It is evaluated by overilluminating a limited part of the image zone at an exposure of N times E_{SAT} and observing how far the bright spot extends from the initially illuminated zone.

With overillumination, three parameters are to be considered :

- blooming
- smearing effect
- crosstalk

a) Blooming :

Antiblooming effect is measured on area arrays by applying $2 \times E_{SAT}$ on 10 % of picture height and checking that spreading is limited to 10 % of E_{SAT} on the third line following the illuminated zone. Measurement is made under specified light illumination conditions, and characterizes the intrinsic antiblooming efficiency, which is unlimited.

b) Smearing effect

This is due to the passage of each column pixel along the overilluminated element(s) during the image to memory zone transfer. It is thus dependent only on image to memory zone transfer frequency for a given overillumination ; it is independent of wavelength.

c) Crosstalk effect

This is linked to the probability of collecting an electron generated under one pixel in a neighbouring well.

The antiblooming structure does not directly reduce the crosstalk (or diffusion) effect, which depends on overillumination level and wavelength. This latter characteristic is a function of pixel geometry and substrate structure.

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