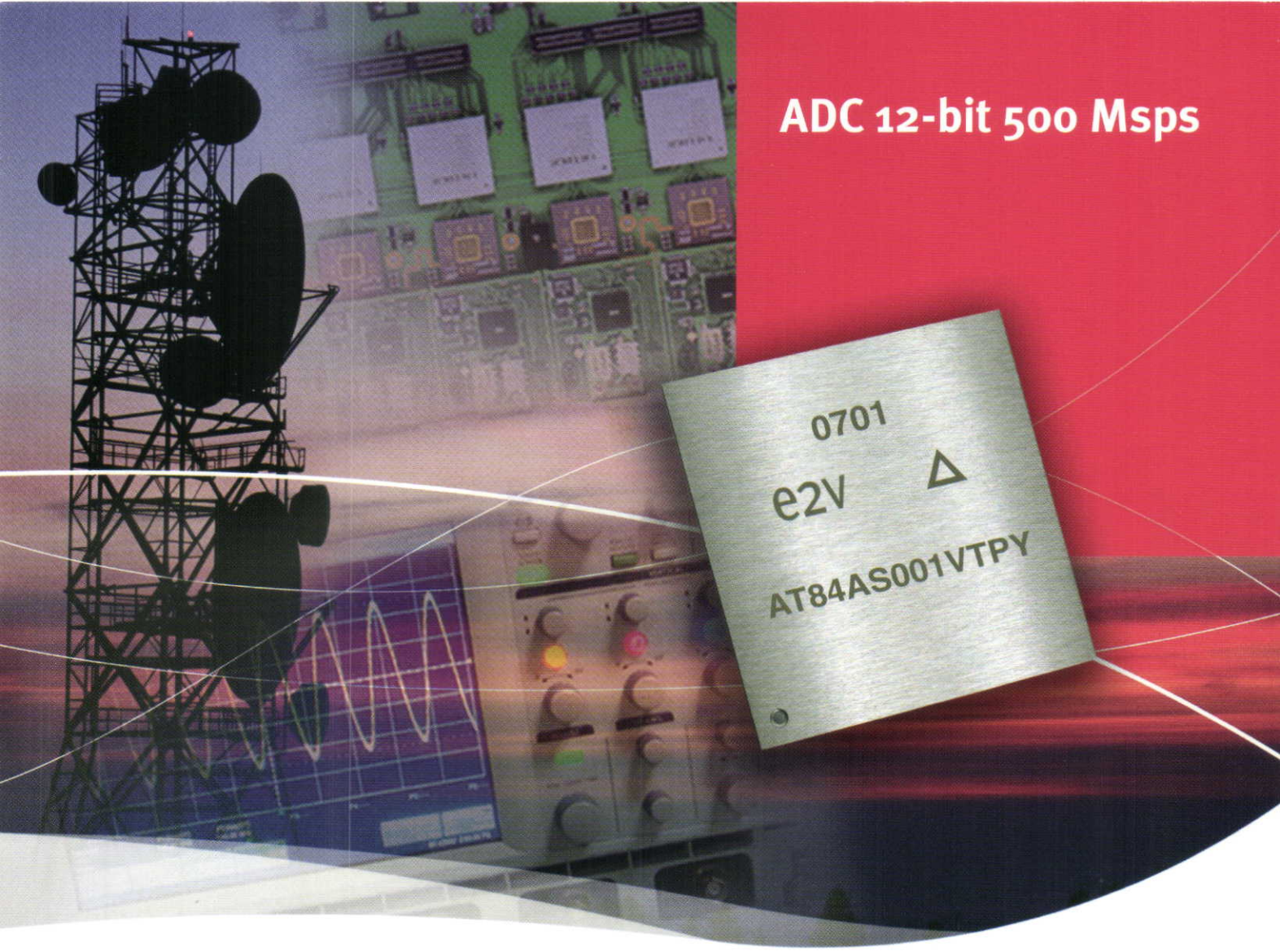

The world's fastest monolithic 12-bit Analogue to Digital Converter

Key performance/features

- True single core ADC, 500 Msps
- Gain and offset adjustments via SPI to make interleaving possible
- 1Vp-p input voltage range; choice of balun or amplifier as input driver
- No pipeline architecture = no long pipeline delay
- Max bit error rate: 10^{-14}
- No heatsink/thermal pad required
- No warm-up, no calibration

Applications

- Telecom test equipment (3G, WiMax, wireless LAN)
- Telecom base stations (E-band Microwave links)
- ATE test equipement (semiconductor, speciality industrial)
- Military (radar, ECM)
- Speciality high energy physics
- Laser measurement
- Data acquisition board
- Software defined radio systems
- All-in-one scope & spectrum analyser

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e2v

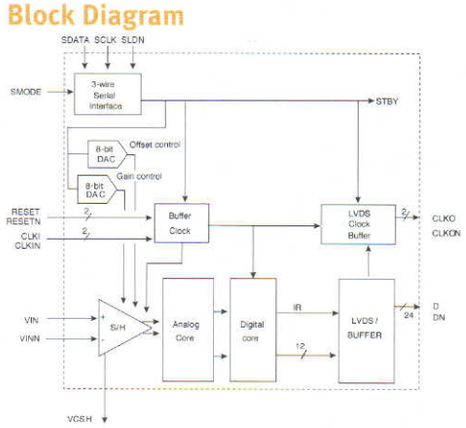
ADC 12-bit 500 Msps

A feature rich 12-bit 500 Msps ADC with true single core guarantee.
Input Gain and Offset can be adjusted on the fly by software via the SPI interface.
The input voltage range allows for a broader choice of analogue front-end circuitry, even DC coupling from DC to 500 MHz is possible with industry standard high speed amplifiers.
This opens the way for 2-in-1 data acquisition boards featuring both DC coupled time domain analysis and frequency domain analysis, at the same time, with the same hardware.
Enjoy the very short latency of e2v's non-pipeline ADC architecture.

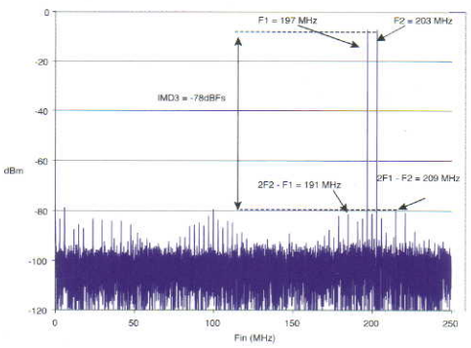
Power up and go! Forget stand-by modes, simply power on and off, enjoy performance at low power without compromise.
For applications that do not require continuous sampling, e2v's true single core ADC technology makes it possible to really reduce the average power consumption, by keeping T_{on} to a very low minimum in the following equation:
$P_{average} = P_{nominal} \times (T_{on} / (T_{off} + T_{on}))$.

T_{on} is only limited by the power supply voltage stabilisation time and the minimum sampling time required by the application, this can be as low as a few milliseconds in the case of pulsed signals. By comparison, competing ADCs with internal interleaving require T_{on} to be in the order several seconds, the difference can be as high as a factor of 1000.

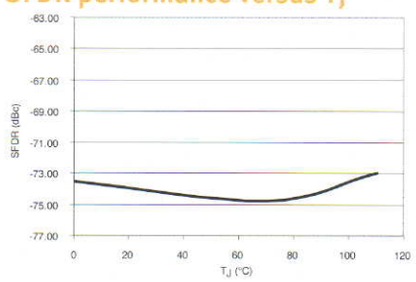
Block Diagram



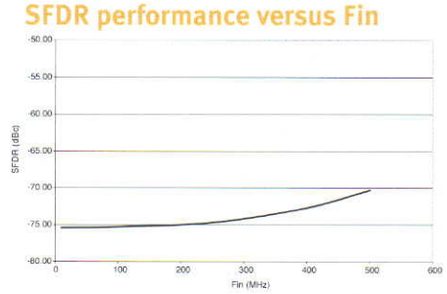
Dual tone 203 MHz



SFDR performance versus Tj



SFDR performance versus Fin



Key specifications

P/N	Resolution	Speed	Input BW	SFDR	SNR	ENOB	BER	Latency	Package	Temp. range
AT84AS001	12 bits	500 Msps	1 GHz	75 dBc	62 dB	10 bits	10E-14	5 nsec	EBGA	Commercial
				@ 250 MHz	@ 250 MHz		@ full speed	no pipeline, ideal for real time systems	enhanced ball grid array	no need for heatsink/ thermal pad

Comments

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