



Quad 8-bit 1.25 Gsps

The ADC which combines the 8-bit speed world record with full flexibility

Key performance/features

- Quad ADC with 8-bit resolution
 - 1.25 Gsps sampling rate in four-channel mode
 - 2.5 Gsps sampling rate in two-channel mode
 - 5 Gsps sampling rate in one-channel mode
 - Built-in four by four cross-point switch
- Fully interleavable via on-chip channel management
- Digital interface (SPI) with reset signal
- Gain, offset, fine clock phase adjustment on the fly
- Single master clock input for all operating modes
- Selectable 2 GHz, 1.5 GHz, 600 MHz, 500 MHz Full power input bandwidth (-3 dB)
- Power dissipation: 1 W per Channel

Applications

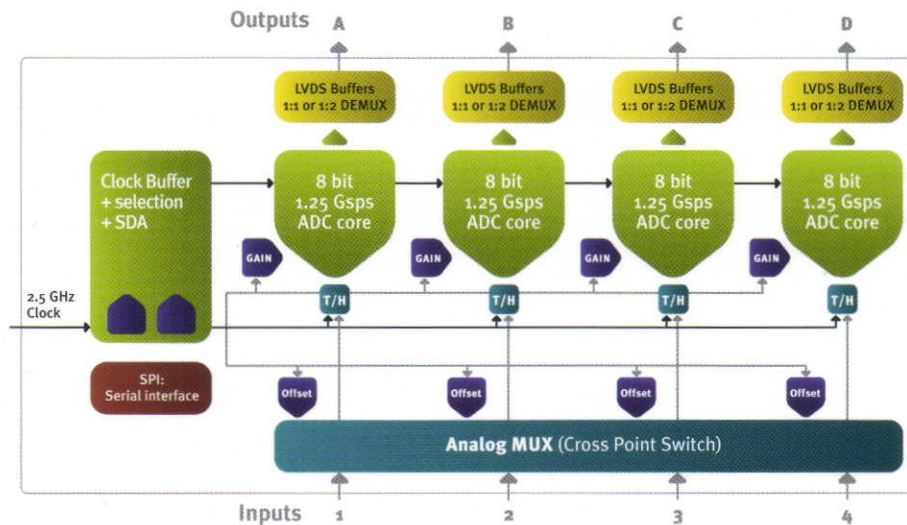
- Digital oscilloscopes
- ATE (Automated Test Equipment)
- Data storage
- Scanners (bar code readers)
- Military (radar, ECM)
- Specialty high speed physics
- Lidar
- DAB, VME, PCI
- Radio astronomy

One device integrating four cores running at 1.25 Gsps each.
Interleavable either to 2 x 2.5 Gsps or to 1 x 5 Gsps.
No hidden interleaving inside each core.

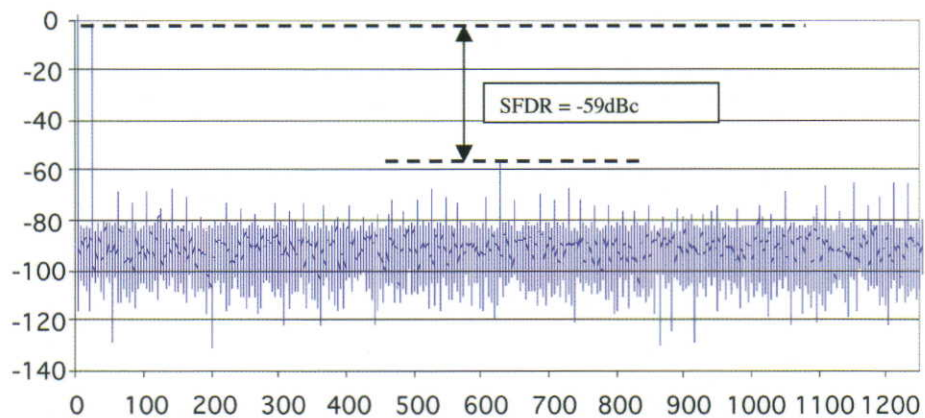
Many SPI features which can be changed on the fly, including a true cross point switch, selectable operation modes, programmable input bandwidth, input gain adjustment, input offset adjustment, fine clock phase adjustment and selectable output DMUX ratio.

All that is backed by the very short latency of e2v's non-pipeline ADC architecture.

Quad 1.25 Gsps
(EV8AQ16oCTPY)
Block diagram



FFT spectrum



Key specifications

| Operation | Resolution | Channel | Speed | SFDR | ENOB | SNR | Comments |
|-----------|------------|---------|----------|--------|----------|---------|---------------|
| 4x1 mode | 8 bits | 4 | 1.25 GHz | 56 dBc | 7.3 bits | 45 dB | @ 620 MHz Fin |
| 2x2 mode | 8 bits | 2 | 2.5 GHz | 56 dBc | 7.2 bits | 44.5 dB | @ 620 MHz Fin |
| 1x4 mode | 8 bits | 1 | 5 GHz | 56 dBc | 7.1 bits | 44 dB | @ 620 MHz Fin |

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